Remarks

Reconsideration of this application is respectfully requested.

Upon entry of the foregoing amendment, claims 47, 53, 67, 72 and 79-82 are pending in the application, with 47, 67 and 79-82 being the independent claims. Claims 41-46, 48-52, 54-66, 68-71 and 73-78 are sought to be cancelled without prejudice to or disclaimer of the subject matter therein. Claims 47, 53, 67 and 72 have been amended. New independent claims 79-82 have been added to replace allowable dependent claims 48, 52, 68 and 71, respectively, including the features of their respective base claims. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Examiner Interview

Applicants and Applicants' representative wish to thank Examiner Donaghue for conducting the personal interview with Applicants' undersigned representative on January 24, 2002. The Examiner Interview Summary Record accurately reflects the substance of the interview.

Rejections and Amendments

In the Office Action dated March 15, 2002, claims 47, 48, 52, 53, 67, 68, 71 and 72 were "objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." Accordingly, by way of the above Amendments, Applicants have placed these claims in independent form. To expedite issuance of the allowed claims, the rejected claims are being cancelled without prejudice or disclaimer. Applicants reserve the right and hereby give notice of their intent to pursue those claims and traverse the rejection in a continuation application, which will be filed in due course.

In conclusion, Applicants respectfully request that the allowed claims be passed to issue and that the rejections be withdrawn as moot in light of the cancellation of the rejected claims.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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Version with markings to show changes made

Claims 41-46, 48-52, 54-66, 68-71 and 73-78 have been cancelled.

47. (Once Amended) [The method as recited in claim 42,] A computer-based method for providing extended precision in single instruction multiple data (SIMD) arithmetic operations, comprising the steps of:

(a) loading a first vector into a first register, said first vector comprising a plurality of N-bit elements;

(b) loading a second vector into a second register, said second vector comprising a plurality of N-bit elements;

(c) executing an arithmetic instruction for at least one pair consisting of an N-bit element in said first register and an N-bit element in said second register, to produce a resulting element;

(d) writing said resulting element into an M-bit element of an accumulator, wherein M is greater than N;

(e) transforming said resulting element in said accumulator into a width of N-bits; and

(f) writing said resulting element into a third register;

wherein said accumulator comprises a plurality of M-bit elements and wherein steps (c)-(f) operate on a plurality of elements of said first and second vectors to produce a resultant vector formed from a plurality of resulting elements written to said third register; and

wherein said resulting elements in said accumulator are wrapped around the representable range of said resulting elements.

53. (Once Amended) The method as recited in claim [52] 80, wherein said rounding step comprises one of:

rounding said resulting element towards zero;

rounding said resulting element towards the nearest unit, wherein said resulting element is rounded away from zero if said resulting element is at least halfway towards the nearest unit; and

rounding said resulting element towards the nearest unit, wherein said resulting element is rounded towards zero if said resulting element is at least halfway towards the nearest unit.

67. (Once Amended) [The system as recited in claim 63,] A processor for providing extended precision in single instruction multiple data (SIMD) arithmetic operations, comprising:

means for executing an arithmetic instruction involving an element of a first vector and an element of a second vector to produce a resulting element, said first and second vector comprising a plurality of N-bit elements;

an accumulator for receiving said resulting element, wherein said resulting element is stored in an M-bit element of said accumulator and wherein M is greater than N;

means for transforming said resulting element in said accumulator into a width of N-bits; and

means for writing said transformed resulting element to a register;

wherein said accumulator comprises a plurality of M-bit elements and wherein said means for executing is repeated for said plurality of elements of said first and second vectors to produce a plurality of resulting elements that are received by said accumulator and wherein said means for transforming and said means for writing are performed on said plurality of resulting elements; and

wherein said resulting elements in said accumulator are wrapped around the representable range of said resulting elements.

72. (Once Amended) The processor as recited in claim [71] 82, wherein said rounding means comprises one of:

means for rounding said resulting element towards zero;

means for rounding said resulting element towards the nearest unit, wherein said resulting element is rounded away from zero if said resulting element is at least halfway towards the nearest unit; and

means for rounding said resulting element towards the nearest unit, wherein said resulting element is rounded towards zero if said resulting element is at least halfway towards the nearest unit.

New claims 79-82 have been added.